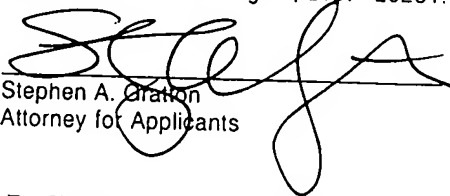


CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Express Mail No.: ET 203 391 629US
Date of Deposit: June 24, 2002

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Address" Service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner of Patents, Box Patent Application, Washington, D.C. 20231.

June 24, 2002
Date of Signature


Stephen A. Gratton
Attorney for Applicants

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

NO FLOW UNDERFILL MATERIAL AND
METHOD FOR UNDERFILLING
SEMICONDUCTOR COMPONENTS

INVENTOR

TONGBI JIANG

ATTORNEY'S DOCKET 01-0219

Field of the Invention

This invention relates generally to semiconductor packaging, and more particularly to a no flow underfill material for underfilling semiconductor components. This invention also relates to a method for underfilling semiconductor components using the underfill material, and to electronic systems constructed using the underfill material.

Background of the Invention

Semiconductor components, such as packages, dice and wafers include terminal contacts which provide input/output paths to the integrated circuits contained on the components. For surface mount components, the terminal contacts can comprise solder or gold bumps or balls, bonded to contact pads on the component. For some components, such as chip scale packages, BGA packages, and flip chip devices, the terminal contacts can be arranged in a dense grid array, such as a ball grid array (BGA), or a fine ball grid array (FBGA).

One method for attaching components having this type of terminal contacts into various electronic systems is known as flip chip bonding. With flip chip bonding the terminal contacts on the component are bonded to corresponding substrate contacts on a supporting substrate, such as a module substrate or a printed circuit board (PCB). A typical bonding process involves reflowing terminal contacts made of solder or gold to form metallurgical bonds with the substrate contacts.

One aspect of flip chip mounted components is that thermal stresses can develop at the connections (e.g., solder joints) between the terminal contacts and the substrate contacts. These thermal stresses develop because the components are formed of a first type of material (e.g., silicon), the terminal contacts are formed of a second type of material (e.g., solder or gold), and the substrate is formed of a third type of material (e.g., ceramic or bismaleimide triazine). The different materials have

different thermal coefficients of expansion (TCE), such that variations in temperature cause the materials to expand and contract by different amounts.

These thermal stresses can cause fatigue fractures to develop at the connections. The fatigue fractures can affect the reliability of the connections, and the physical bond between the component and the substrate. In addition, fatigue fractures can cause some of the connections to fail entirely. For example, failures from fatigue fractures often occur at the outside corners of a grid array where the stresses are most concentrated.

One method for alleviating the adverse affects of thermal stresses is to encapsulate the terminal contacts in a low stress underfill encapsulant. Typically, the underfill encapsulant also completely fills the space between the component and the substrate. The underfill encapsulant functions to redistribute the thermal stresses over a surface area that is about the same size as the component. In addition, the TCE of the underfill encapsulant can be closely matched to the TCE of the terminal contacts, such that thermal stresses at their connections with the substrate contacts are reduced. The underfill encapsulant also physically bonds the component to the substrate, and protects the terminal contacts from contaminants, such as moisture and dust.

Two different processes have been developed in the art for encapsulating components in an underfill encapsulant. A capillary underfill process is shown in Figure 1A. A no flow underfill process is shown in Figure 1B. Either of these processes can be performed at the wafer level on wafer sized components (e.g., semiconductor wafers), or at the die level on die sized components (e.g., semiconductor packages).

Referring to Figure 1A, the capillary underfill process includes four steps (Steps A-D). Initially, a component 10 and a supporting substrate 12 are provided. The component 10 includes terminal contacts 14, and the supporting substrate

12 includes substrate contacts 16, substantially as previously described. Step A is an alignment step, in which the terminal contacts 14 are aligned with the substrate contacts 16. Step B is a bonding step, such as a solder reflow, in which the terminal contacts 14 are bonded to the substrate contacts 16. Step C is a capillary injection step, in which a dispensing apparatus 18 dispenses viscous underfill material 20 which is drawn by capillary action between the component 10 and the substrate 12. Step D is a curing step, in which the underfill material 20 is cured to form an underfill layer 22 which encapsulates the terminal contacts 14 and bonds the component 10 to the substrate 12.

As with most processes, the capillary underfill process has certain limitations. For example, voids can form in the underfill layer 22 if the capillary injection step is not performed properly. In addition, the underfill material 20 must have a relatively low viscosity, such that the curing step takes a relatively long time to perform.

Referring to Figure 1B, the no flow underfill process also includes four steps (Steps 1-4). Initially, in Step 1 the substrate 12 and the substrate contacts 16 are provided. Step 2 is a no flow dispensing step, in which a no flow underfill material 20NF is deposited by a dispensing apparatus 18NF onto the substrate contacts 16 and onto the surface of the substrate 12. The no flow underfill material 20NF has a relatively high viscosity, such that it remains on the area of the substrate 12 on which it is initially deposited. Step 3 is a placement step, in which the terminal contacts 14 on the component 10 are pressed through the no flow underfill material 20NF into contact with the substrate contacts 16. Step 4 is a bonding and curing step, in which the terminal contacts 14 are bonded to the substrate contacts 16, and the no flow underfill material 20NF is cured to form a no flow underfill layer 22NF. Because bonding between the terminal contacts 14 and the substrate contacts 16 typically

occurs by solder reflow, the no flow underfill material 20NF is also sometimes referred to as a "reflow" encapsulant.

The no flow underfill process also has certain limitations. For example, the height of the terminal contacts 14 can vary, such that some of the terminal contacts 14 may not physically touch the substrate contacts 16 during the placement step. These terminal contacts 14 may not bond properly to the substrate contacts 16 affecting the physical and electrical connections therebetween. Similarly, the surface of the substrate 12 may be non planar causing the same bonding problem. Also, the no flow underfill material 20NF is difficult to formulate with the required physical properties. For example, polymers with no flow characteristics may not have a good TCE match with the terminal contacts 14, and may have low modulus of elasticity characteristics. Because of these characteristics, no flow underfill layers 20NF fail earlier in temperature cycling tests than capillary underfill layers.

Referring to Figure 1C, another problem associated with no flow underfill processes is illustrated. In this example the terminal contacts 14 comprise a solder material, such as a SnPb solder, that has been reflow bonded to the substrate contacts 16. In addition, the no flow underfill layer 22NF includes a filler which includes non conductive particles 27. For example, the non-conductive particles 27 can comprise silicates configured to reduce the TCE, and to adjust the viscosity of the underfill layer 22NF. As shown in Figure 1C, some of the non-conductive particles 27 can be trapped at the interface of the terminal contacts 14 with the substrate contacts 16. These trapped non-conductive particles 27 can add resistance to the electrical connections between the terminal contacts 14 and the substrate contacts 16. In addition, these trapped non-conductive particles 27 can adversely affect the physical bond between the terminal contacts 14 and the substrate contacts 16.

Referring to Figure 1D, another problem associated with no flow underfill processes is illustrated. In this example the terminal contacts 14 are made of gold, and have again been bonded to the substrate contacts 16. In addition, the
5 no flow underfill layer 22NF includes Ni particles 29. As before, some of the Ni particles 29 can be trapped at the interface of the terminal contacts 14 with the substrate contacts 16. These Ni particles 29 have a different resistivity than the gold terminal contacts 14, such that the
10 resistance of the electrical connections between the terminal contacts 14 and the substrate contacts 16 can vary, and change abruptly across the terminal contacts 14. In addition, the Ni particles 29 can adversely affect the physical bond between the terminal contacts 14 and the
15 substrate contacts 16.

The present invention provides a no flow underfill material, and a method of underfilling, that overcome some of the limitations of conventional underfill processes.

20 Summary of the Invention

In accordance with the present invention, a no flow underfill material, a method for underfilling semiconductor components on supporting substrates using the underfill material, and an electronic system incorporating the
25 underfill material, are provided.

The underfill material is formulated to cure, or polymerize, into an underfill layer for encapsulating electrical connections between solder terminal contacts on the semiconductor component, and substrate contacts on the
30 substrate. The underfill material includes an electrically insulating polymer base material, such as an epoxy resin, a silicone resin, or a polyimide resin. The polymer base material is formulated to have a viscosity that provides no flow characteristics over a first temperature range. In
35 addition to the polymer base material, the underfill material includes a curing agent or hardener, such as a reactant or a

solvent, that reacts with and cures the polymer base material. In addition, the underfill material includes a fluxing agent, such as an acid, that removes surface oxides from the substrate contacts.

5 The underfill material also includes electrically conductive micro particles embedded in the polymer base material. The micro particles can comprise a solder alloy (e.g., eutectic SnPb), or another conductive material (e.g., Sn), configured to melt at a second temperature range, and to
10 alloy with the solder terminal contacts to form reinforcing solder layers on the electrical connections. In addition, the concentration of the micro particles in the polymer base material is selected such that there is no electrical conductivity through the cured underfill layer in the X and Y
15 directions.

 The method includes the steps of providing the component with the terminal contacts, and providing the supporting substrate with the substrate contacts. The method also includes the step of providing the underfill material with
20 the electrically conductive micro particles embedded in the polymer base material. In addition, the method includes the steps of depositing the underfill material on the substrate (or alternately on the component), placing the terminal contacts in contact with the substrate contacts while the
25 underfill material is in a viscous condition, bonding the terminal contacts to the substrate contacts to form the electrical connections, and then curing the underfill material to form the underfill layer.

 The bonding and curing steps can be initiated at the
30 same time at the second temperature range using a standard reflow furnace. Preferably, the electrical connections are formed before the underfill layer is completely cured. During the bonding and curing steps, at least some of the micro particles can alloy with the terminal contacts and form
35 solder layers bonded to the substrate contacts.

The method can be performed at the wafer level on a wafer sized component (e.g., a semiconductor wafer) or at the die level on a die sized component (e.g., a semiconductor die or a semiconductor package). A wafer level method can also
5 include a singulating step in which the wafer sized component is separated into die sized components. In addition, some of the steps can be performed at the wafer level, while other steps are performed at the die level. For example, the underfill material can be deposited on a wafer containing a
10 plurality of dice or packages. Next, a singulating step can be performed to singulate the wafer into dice or packages. The individual dice or packages can then be attached to the substrate while the underfill layer remains in a viscous condition, or is placed in a B-stage condition.

15 The electronic system includes at least one component on a substrate, and a plurality of electrical connections between the terminal contacts on the component and substrate contacts on the substrate. The system also includes an underfill layer attaching the component to the substrate and
20 encapsulating the electrical connections. In addition, the underfill layer includes a plurality of conductive particles, at least some of which form solder layers bonded to the substrate contacts.

25 Brief Description of the Drawings

Figure 1A is a schematic view illustrating steps in a prior art capillary underfill process;

Figure 1B is a schematic view illustrating steps in a prior art no flow underfill process;

30 Figure 1C is an enlarged cross sectional view taken along section line 1C-1C of Figure 1B illustrating non conductive particles in a no flow underfill layer;

Figure 1D is an enlarged cross sectional view equivalent to Figure 1C illustrating nickel particles in a no flow
35 underfill layer;

Figures 2A-2E are schematic cross sectional views illustrating steps in the method for underfilling semiconductor components in accordance with the invention;

5 Figure 3A is an enlarged cross sectional view taken along section line 3A-3A of Figure 2B illustrating the no flow under fill material of the invention;

10 Figure 3B is an enlarged cross sectional view taken along section line 3B-3B of Figure 2D illustrating a terminal contact on a substrate contact during a placement step of the method;

Figure 3C is an enlarged cross sectional view taken along section line 3C-3C of Figure 2D illustrating a terminal contact spaced from a substrate contact during the placement step of the method;

15 Figure 3D is an enlarged cross sectional view taken along section line 3D-3D of Figure 2E illustrating a terminal contact/electrical connection prior to completion of a bonding step;

20 Figure 3E is an enlarged cross sectional view taken along section line 3E-3E of Figure 2E illustrating the electrical connection following the bonding step;

Figure 3F is a cross sectional view taken along section line 3F-3F of Figure 2E illustrating the cured underfill layer;

25 Figure 4 is a schematic cross sectional view equivalent to Figure 2C but illustrating an alternate embodiment of the method shown in Figures 2A-2E;

30 Figure 5A is a plan view of a system constructed in accordance using the underfill material and method of the invention; and

Figure 5B is a cross sectional view taken along section line 5B-5B of Figure 5A.

Detailed Description of the Preferred Embodiments

35 As used herein, the term "semiconductor component" refers to an electronic element that includes a semiconductor

die. Exemplary semiconductor components include semiconductor packages, semiconductor dice, BGA devices, flip chip devices and semiconductor wafers.

Referring to Figures 2A-2E, and Figures 3A-3F, a method
5 for underfilling a semiconductor component 28 (Figure 2C) on a supporting substrate 32, using a no flow underfill material 30 (Figure 2B) formulated in accordance with the invention is illustrated. In addition to underfilling the component 28, the method encapsulates and attaches the component 28 to the
10 substrate 32.

Referring to Figure 2A, the substrate 32 can comprise a module substrate, a circuit board, a package substrate, or any other element for mounting one or more semiconductor components 28 in a desired electrical configuration. In
15 addition, the substrate 32 can comprise an electrically insulating material, such as ceramic, or plastic (e.g., bismaleimide triazine (BT), polyimide resin), or a semiconductor material, such as silicon. Further, the substrate 32 can have a selected peripheral size, shape and
20 thickness and can be configured to mount one or more components 28.

The substrate 32 includes a plurality of substrate contacts 34, which in the illustrative embodiment comprise planar pads. The substrate contacts 34 are arranged in a
25 pattern that matches a pattern of terminal contacts 36 (Figure 2C) on the semiconductor component 28 (Figure 2C). For example, the substrate contacts 34 and the terminal contacts 36 can be arranged in a dense grid array, such as a micro grid array. Also in the illustrative embodiment, the
30 terminal contacts 36 comprise a solder alloy, and the substrate contacts 34 comprise a solder wettable metal.

Suitable solder alloys for the terminal contacts 36 include eutectic PbSn solder alloys, such as 95%Pb/5%Sn, 60%Pb/40%Sn, 63%Sn/37%Pb and 62%Pb/36%Sn/2%Ag. In general,
35 these eutectic solder alloys melt at a temperature of between about 150 °C to 250 °C. As another alternative, the terminal

contacts 36 can comprise a Pb free solder alloy, such as a SnAgCu solder.

Suitable metals for the substrate contacts 34 include copper, tin, lead, palladium, platinum, nickel, chrome, titanium, gold, zinc and alloys of these metals. As will be further explained, the method of the invention forms electrical connections 46 (Figure 2E) which physically and electrically connect the component 28 to the substrate 32. In addition, the method of the invention forms solder layers 52 (Figure 3E) between the terminal contacts 36 and the substrate contacts 34 which reinforce the electrical connections 46.

A peripheral outline and size of the substrate contacts 34 can be selected as required (e.g., circular, square, polygonal). The substrate contacts 34 are in electrical communication with conductors (not shown), and various other electronic elements (not shown) on the substrate 32. Further, the substrate 32 can include multiple patterns of substrate contacts 34, such that multiple components 28 (Figure 2B) can be attached to the substrate 32. For example, for a wafer sized component (e.g., semiconductor wafer), the substrate 32 can include enough patterns of substrate contacts 34 to electrically engage all of the dice on the component.

The substrate 32 can also include a mask 38, such as a solder mask, having openings 40 aligned with the substrate contacts 34. The mask 38 can comprise an electrically insulating material, such as a photoimageable resist, configured to provide electrical insulation, and to prevent electrical shorting.

Initially, as shown in Figure 2B, the underfill material 30 is deposited on a selected area of the substrate 32, and covers the substrate contacts 34 in this area. The underfill material 30 has a peripheral outline that is about the same as the peripheral outline of the component 28. In addition,

a thickness T of the underfill material 30 is about the same as a height H1 (Figure 2C) of the terminal contacts

The underfill material 30 can be deposited using a suitable deposition process, such as positive displacement through a nozzle, screen printing, stenciling or pin transfer. Systems are commercially available for performing each of these processes in the context of semiconductor packaging. For example, material dispensing systems are manufactured by Asymtek of Carlsbad, CA, and by Camalot of Cookson, UK.

The underfill material 30 is formulated to meet environmental standards recognized in the semiconductor industry. In addition, the underfill material 30 is formulated with a viscosity that provides non-flowing characteristics over a selected temperature range, such as a room temperature range (e.g., 22°C to 37.8°C) or an elevated temperature range (e.g., 22°C to 100°C). This viscosity allows the underfill material 30 to maintain a desired size and shape, and to remain on the selected area of the substrate 32 over the selected temperature range. By way of example, the underfill material 30 can have a viscosity at a temperature between 22°C to 100°C., of about 7000 to 200,000 cps (centipoise). In this case, the viscosity can be measured using a Brookfield Viscosity with a spindle 51 rotated at about 5 rpm.

The underfill material 30 can also be formulated for deposition at a first viscosity followed by semi curing to a second viscosity. For example, the underfill material can initially be deposited with a first viscosity, and then partially cured to a second viscosity, such as a B-stage condition. As used herein, the term B-stage condition refers to a semi cured condition in which the underfill material is still viscous or pliable, but possesses a structural rigidity. The B-stage condition can occur at ambient temperature over a certain time period, or can be achieved by semi curing at a selected temperature and time period.

As a primary constituent, the underfill material 30 includes an electrically insulating polymer base material 44 (Figure 3A) such as an epoxy resin, a silicone resin, a polyimide resin, or a similar elastomeric material having suitable non-flowing and curable properties. By way of example, specific polymer resins include, but are not limited to: phthalate-acetate hydroxyl copolymer, dibutyl isobutyl diphenol cellulose copolymer, and butyl phenol ketyl vinyl acetate polymer. One specific commercial polymer resin that can be used as the polymer base material 44 is manufactured by Dexter Electronic Materials of Rocky Hill, CT under the trademark "HYSOL" FF2000.

The underfill material 30 also includes a curing agent or hardener, such as a reactant or a solvent, that reacts with and cures the polymer base material 44 over the selected temperature range and during a selected time period. Suitable curing agents include amines, anhydrides, and butyl carbitol acetate. By way of example, the curing agent can be included in the polymer base material 44 in a quantity sufficient to cure the polymer base material 44 at temperatures and in time periods used during a solder reflow process for flip chip bonding semiconductor components to substrates. The curing step can be performed simultaneous with a bonding step using a reflow furnace to be hereinafter described. If required, a final cure can also be performed at a lower temperature for a longer time period.

The underfill material 30 also includes a fluxing agent configured to clean and remove oxides from the substrate contacts 34. Suitable fluxing agents include carboxylic acid, abietic acid, citric acid, 2-furoic acid, malic acid and polyacrylic acid.

As shown in Figure 3A, the underfill material 30 also includes a plurality of electrically conductive micro particles 42 embedded in the polymer base material 44. The micro particles 42 function as a filler which strengthens and increases the electrical conductivity of the electrical

connections 46 (Figure 2E). Preferably, the micro particles 42 comprise a metal that melts at the same temperature as the terminal contacts 36 (Figure 2C) on the component 28. In addition, the micro particles 42 preferably comprise a metal
5 that alloys with the terminal contacts 36 to form the solder layer 52 (Figure 3E).

One suitable metal for the micro particles 42 is a solder alloy. For example the micro particles 42 can comprise the same solder alloy as the terminal contacts 36,
10 such as the previously described PbSn, PbSnAg and SnAgCu solder alloys. The micro particles 42 can also comprise a different solder alloy than the terminal contacts, provided the melting temperatures are similar. As another alternative, the micro particles can comprise a metal, such
15 as Sn, Pb, Ag, Au, Ge, Cu or In, that alloys easily with the solder alloy of the terminal contacts 36.

The micro particles 42 can have any shape, such as spherical, cigar, snow flake or dendritic. The outside diameter of the micro particles can be less than about 10 μm ,
20 and preferably less than about 5 μm . A representative size range can be from 1 μm to 10 μm . In addition, the micro particles 42 are present in the polymer base material 44 in a relatively low concentration, which prevents electrically conductivity in a first direction (X direction), and also in
25 a second orthogonal direction (Y direction). As shown in Figure 3A, the X and Y directions are located along planes that are generally parallel to the substrate contacts 34 (Figure 2B) and generally perpendicular to a longitudinal axis of the terminal contacts 36.

30 The micro particles 42 preferably have a concentration in the underfill material 30, expressed as a volume percentage, of less than about 50% and more preferably less than about 30%. A representative range for the micro particles 42 can be from about 10% to 50%, where the
35 percentages represent a volume percentage of the total volume of the underfill material 30.

Referring to Figure 2C, an alignment step is performed in which the terminal contacts 36 on the component 28 are aligned with the substrate contacts 34 on the substrate 32. The alignment step can be accomplished using techniques that
5 are known in the art, such as optical alignment using optical viewing devices, or mechanical alignment using fixtures and jigs.

The terminal contacts 36 are in electrical communication with the integrated circuits and other electronic devices
10 contained on the component 28, and provide input/output connections for the component 28. In the illustrative embodiment, the terminal contacts 36 comprise solder bumps or balls that have been formed on pads 48 on the component 28 using techniques that are known in the art (e.g., reflow
15 bonding, solder ball bumping). Further, the number, the diameter D, the height H, and the pitch P of the terminal contacts 36 can be selected as required. A representative diameter D and height H can be from about 0.005-in (0.127 mm) to about 0.016-in (0.400 mm) or larger. A representative
20 pitch P can be from about 0.004-in (0.100 mm) to about 0.039-in (1.0) mm or more.

As shown in Figure 2C, the terminal contacts 36 may not all have a uniform height. For example, the terminal contact 36 on the outer right edge of the component 28 may have a
25 height H1 that is greater than a height H2 of an adjacent terminal contact 36 ($H1 > H2$). As will be further explained, during formation of the electrical connections 46 (Figure 2E), the underfill material 30 functions to alleviate the affects of this height differential.

Following the alignment step, a placement step is performed. As shown in Figure 2D, during the placement step the terminal contacts 36 on the component 28 are pushed
30 through the underfill material 30, such that the terminal contacts 36 physically touch the substrate contacts 34 on the substrate 32. The placement step, and the alignment step as well, can be performed using an automated system, such as one
35

manufactured by Datacon of Austria under the trademark "2200 APM".

As shown in Figure 3B, the ideal situation is to have the terminal contacts 36 in metal to metal contact with the substrate contacts 34. However, even with metal to metal contact, some underfill material 30 is trapped between the terminal contacts 36 and the substrate contacts 34. This trapping phenomena occurs with the curved topography of the terminal contacts 36, and with adherence of the underfill material 30 to the terminal contacts 36.

In addition, as shown in Figure 3C, a terminal contact 36 can be spaced from its corresponding substrate contact 34 by a gap S. This gap S may be due to the previously described height differential between the terminal contacts 36, or may be due to the non-planarity of the substrate contacts 34. As also shown in Figure 3C, underfill material 30 is present in the gap S due to the initial deposition of the underfill material 30 on the substrate contacts 34.

Following the placement step, and as shown in Figure 2E, a bonding step which forms the electrical connections 46, and a curing step which forms a cured underfill layer 50 are performed. Although these steps are initiated at the same time, the curing step preferably continues for a time period that is longer than the bonding step.

To initiate the bonding step and the curing step, the component 28 and the substrate 32 are placed in a furnace, such as a commercial reflow furnace. The furnace is maintained at a temperature sufficient to reflow the solder material of the terminal contacts 36. The bonding step and the curing step can be performed using a staged process including a preheat stage (e.g., 120°C to 150°C for 1-5 minutes), a reflow stage (e.g., 150°C to 250 °C for 1-5 minutes), and if necessary a curing stage (e.g., 100°C for 1-20 minutes). Using a staged process, the electrical connections 46 are preferably formed during the reflow stage. Also during the reflow stage and the subsequent curing stage

if performed, the underfill material 30 cures by outgassing or reaction of the curing agent.

Referring to Figures 3D and 3E, the function of the micro particles 42 during the bonding step, and during formation of the electrical connections 46, is illustrated. Figure 3D illustrates the terminal contacts 36 and electrical connections 46 at the start of the bonding step. Figure 3E illustrates the electrical connections 46 at the completion of the bonding step.

As shown in Figure 3D, some of the micro particles 42 are in contact with both the terminal contacts 36/electrical connections 45 and the substrate contacts 34. During the bonding step these micro particles 42 melt into the liquid phase, and alloy with the solder material that forms the terminal contacts 36. In addition, as shown in Figure 3E, the melted micro particles 42 form solder layers 52 that rigidify the completed electrical connections 46, and the metallurgical bonds between the electrical connections 46 and the substrate contacts 34. Similarly, melted micro particles 42 can form in the underfill material 30 located in the spaces S (Figure 3C) and form solder layers 52 in the spaces S.

In addition to rigidifying the electrical connections 46, the melted micro particles provide electrical conductivity in the Z direction (e.g., in a direction parallel to a longitudinal axis of the electrical connections 46). This improves the electrical path from the substrate contacts 34 to the electrical connections 46.

Further, as shown in Figure 3F, the electrical connections 46 are encapsulated in the underfill layer 50. The underfill layer 50 thus rigidifies and seals the electrical connections 46. The underfill layer 50 also seals the space between component 28 and the substrate 32, and physically bonds the component 28 to the substrate 32.

Referring to Figure 4, an alternate embodiment of the method is illustrated. In the alternate embodiment, the

underfill material 30 is initially deposited on the component 28 rather than on the substrate 32. As shown in Figure 4, the underfill material 30 has a thickness that is greater than the height of the terminal contacts 36, such that the terminal contacts are encapsulated by the underfill material 30. Following this deposition step, an alignment step, a placement step, a bonding step and a curing step can be performed, substantially as previously described, to form the electrical connections 46 (Figure 3E), the solder layers 52 (Figure 3E) and the cured underfill layer 50 (Figure 3E).

The alternate embodiment method can be performed initially at the wafer level, such as by depositing the underfill material 30 on a component 28 such as a wafer containing a plurality of components (e.g., dice or packages). The component 28 can then be singulated into a plurality of components and the alignment, placement, bonding and curing steps performed on the individual components, while the underfill material 30 is in a viscous or B-stage condition.

Referring to Figures 5A and 5B, a system 60 constructed using the underfill material 30, and the method of the invention is illustrated. The system 60 comprises a multi chip module configured to perform a desired electrical function (e.g., memory). The system 60 includes a module substrate 32MCM having an edge connector 62, and a plurality of conductors 64 in electrical communication with the edge connector 62. The system 60 also includes a plurality of components 28MCM, such as memory dice or packages, having electrical connections 46MCM formed on substrate contacts 34MCM substantially as previously described. The substrate contacts 34MCM are in electrical communication with the conductors 64 and the edge connector 62. The system 60 also includes an underfill layer 50MCM encapsulating the terminal contacts 36MCM, and attaching the components 28MCM to the substrate 32MCM.

Thus the invention provides an improved underfill material for encapsulating semiconductor components, a method for underfilling semiconductor components using the underfill material, and a system constructed using the underfill
5 material and method. While the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.